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Datasheet
microEnable IV VD1-CL

SMARTER IMAGING FOR BETTER LIVES
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microEnable IV VD1-CL

Product Profile of microEnable IV VD1-CL

Scalable, intelligent image processing board for applications with high data input

- All formats of Camera Link standard
- Suitable for high data input despite of PCIe x1
- Intelligent programming solution
- Multi-device usage
- PCIe x1 for small systems
- Camera Simulator
- Broad support of Third-party software interfaces
- Versatile application and industry usage
- Easy programmable Vision processor for individual realtime funtionality
- Robust and industrial FPGA Technology

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Technical Description

Programmable microEnable IV frame grabber with 2* Camera Link ports (MDR26) for 2*BASE, 1*MEDIUM or 1*FULL (incl. 10-taps) configuration cameras, 256MB DDRRAM acquisition and image processing buffer, PCIe x1 (single lane) PC-interface. Pre-licensed for VisualApplets (Base) and SmartApplets (Base). Documentation, SDK, supporting software tools, functional libraries with acquisition applets and drivers in delivery. Genuine compliance to VisualApplets FPGA programming environment.

Article Details

Product Name	microEnable IV VD1-CL
Match Code	mE4-VD1CL
Article No.	101660
Category	V-Series (image acquisition board)

Device Features

Processor	Vision Processor, Spartan3 FPGA XC3S1600e
On Board Memory	256 MByte DDR-RAM
Processor Board Interface	PixelPlant interface
Data Forwarding	n/a
I/O Module Interfaces	Trigger/GPIO-IF (Opto Trigger, TTL Trigger)

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Camera Interface

Standard	Camera Link 2.0, up to 85 MHz Pixel Clock
Configurations	CL-base, CL-dual base, CL-medium, CL-full, CL-deca (80bit)
Connectors	2* MDR26
Cable Length	standard conform
Power Output	n/a
Camera Support	Area scan camera, line scan camera
Sensor Type	Grayscale sensor, CFA sensor (Bayer), RGB sensor
Sensor Resolution	64k*64k (area scan sensor, VisualApplets), 64k (line scan sensor, VisualApplets)
Bit Depth	8-16-bit (grayscale), 24-48-bit (color)
Data Bandwidth	850 MB/s
Test Environment	Camera Simulator

Controls and General Purpose I/Os

Trigger Board GPIO Interfaces	TTL Trigger board: 8 TTL in and 8 TTL out, max. input freq: 20 MHz; Opto Trigger boards (options): Up to 8 single-ended opto-coupled in (4,5V-28V) or 4 differential opto-coupled in (4,5-28V, RS422 compliant); 8 opto-coupled out (4,5V-28V), max. input freq: 1 MHz
On-board GPIO Interface	n/a
On-board Front GPIO Interface	n/a
Synchronization and Control	Configurable Trigger System supporting several trigger modes (grabber controlled, external trigger, gated, software trigger) and shaft encoder functionality with backward compensation, Multi-Camera-Synchronization
GPIO Summary	8in/8out (max.), TTL or opto-coupled

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Host PC Interface

PC Bus Interface	PCI Express x1 (Gen1)
PC Bus Interface Performance	app. up to 200 MB/s (sustainable)

Physical and Environmental Information

Dimensions	PCIe Standard height, half length card: 167.64 mm length x 111.15 mm height
Approximate Weight	117 g
Power Consumption / Power Source	3.3V, 250 mA / 12V, 520 mA
Operating Temperature	0 - 50°C (32°F - 122°F)
Storage Temperature	-50 - 80°C (-58°F - 176°F)
Relative Humidity	pending
MTBF	176.000 h
Compliances	CE, RoHS, WEEE, REACH

Software

Software Drivers	Windows 7 / 8 (32-bit), Windows 7 / 8 (64-bit), Linux 32-bit, Linux 64-bit
Software Tools	microDisplay (Acquisition control and viewer), microDiagnostics (Service tool), GenICam Explorer (Camera configuration tool), SDK, Documentation, Device Drivers
Software API	Silicon Software SDK, .net interface
FPGA Programming	VisualApplets
BV Software Compatibility	Common Vision Blox, Halcon, LabView, VisionPro, MIL, Sapera, Streampix, SAL3D, 3D Express, Heurisco

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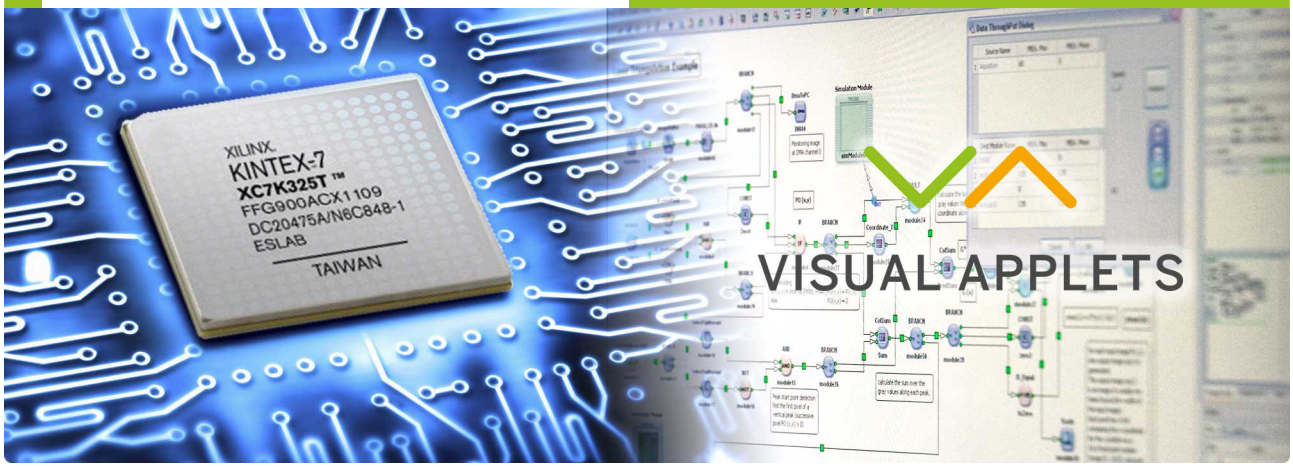

VisualApplets

Often, the goal of industrial image processing applications is to find 100% of all errors and to work in high resolution to identify even the smallest details, to acquire images in the shortest time possible, to detect defects and to forward the results. These tasks frequently require more computing power than a “standard system” can offer. There are solutions that begin the image processing right after the acquisition process but before the camera images are written to storage and taken over by the software.

The processors used in such solutions are designed for image processing. They process data with extremely high parallelism, thus guaranteeing the necessary data throughput. On all its frame grabbers, Silicon Software uses this FPGA technology. In the A-Series (frame grabbers with expanded image recording functions), we have already programmed important and valuable functions that can be activated via the configuration software. For V-Series models (programmable frame grabbers for individual image processing functions), we have released the FPGA for you, as our customer, for individual programming.

To ease your entry into hardware programming, we have developed software that enables you to graphically program FPGAs using data flow diagrams. This program is called VisualApplets.

VisualApplets makes it possible for you to write complex applications on your own, even after a short time, for the special processor. Even without hardware programming expertise. The program is geared toward both software programmers and application engineers. Program in the language of image processors without using hardware code. The simulation works with a rapid image output with which you can immediately check your algorithms and image processing steps.

We have built in many automatic correction functions and generators so that you can concentrate on your actual work. And should an error sneak in, you are immediately made aware of it in color, and solution approaches are offered to you.

An SDK output generates executable example code in C/C++, listing all the parameters (hardware register), in order to control the image processing application out of your software.

What does real time mean? By using FPGA technology, you have a deterministic relationship to the application that works after the start with a constant delay (latency) that is determined by the image processing algorithm. In most cases, this latency lies in the micrometer range.

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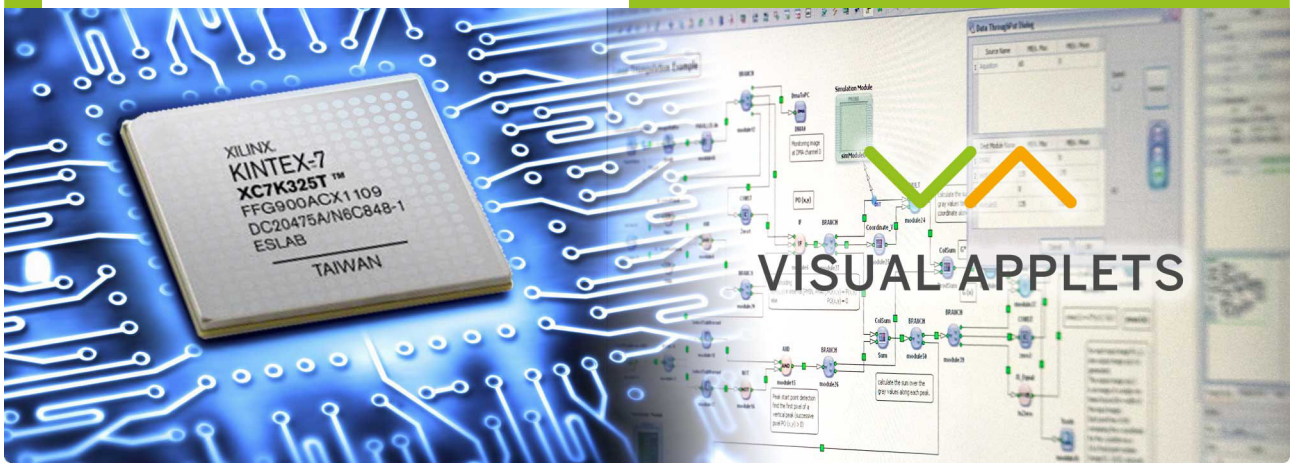

VisualApplets (ctd.)

VisualApplets simplifies image processing programming for you. You can fall back on libraries with over 200 operators. You can create your own libraries for commonly used image processing steps or import them from available hardware code (EDIF over VHDL/Verilog).

With VisualApplets, you acquire a powerful tool that offers you new ways forward for your system solution.

VisualApplets is available for Silicon Software V-Series frame grabbers, including VisualApplets-compatible cameras and imaging devices.

V-Series frame grabbers are already pre-licensed for use with VisualApplets in the basic version. VisualApplets offers several versions of its programming environment; additionally, you can license further operator libraries to expand the range of functions.

In 2006, VisualApplets was honored with the international Vision Award. It has been successfully used in the most diverse industrial applications, both using frame grabbers and in VisualApplets-compatible industrial cameras and image processing devices.

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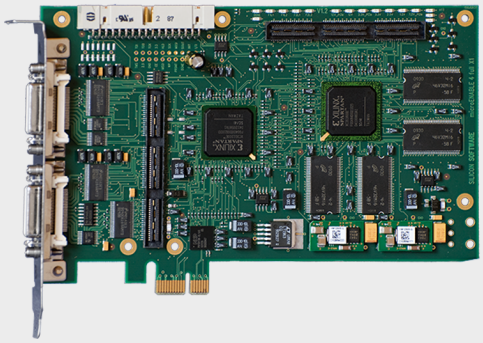
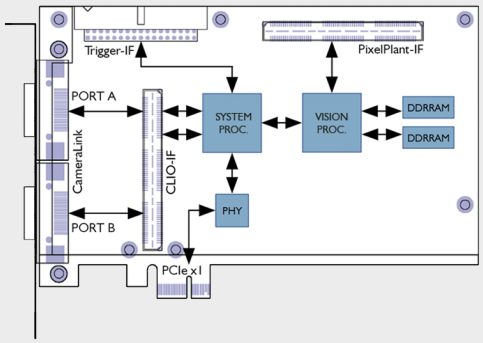
Technical Setup

Board/Housing Measurement





PRODUCT VARIATIONS

microEnable IV AS1-PoCL microEnable IV AD1-CL
microEnable IV AD1-PoCL microEnable IV AD1-mPoCL

PRODUCT EXTENSIONS

Opto-coupled Trigger Board - mE4 (Pull up)Match Code: TRG-OPTO4-PU, Art.No.: 101266 Opto-coupled Trigger Board - mE4 (Pull down)Match Code: RG-OPTO4-PD, Art No.: 101433 Opto-coupled Trigger Board - mE4 (DS Pull up)Match Code: TRG-OPTO4-DSPU, Art No.: 101435 Opto-coupled Trigger Board - mE4 (DS Pull down)Match Code: TRG-OPTO4-DSPD, Art No.: 101437 Opto-coupled Trigger Board - mE4 (DS/SE Pull up)Match Code: TRG-OPTO4-DSSEPU, Art No.: 101443 Opto-coupled Trigger Board - mE4 (DS/SE Pull down)Match Code: TRG-OPTO4-DSSEPD, Art No.: 101444 TTL Trigger Board - mE4Match Code: TRG-TTL4, Art No.: 101248

ORDERING INFO

- microEnable IV VD1-CL,
  mE4-VD1CL, Art No.: 101660

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